

REMARKS

Claims 1-19 are pending in this application. Claims 1-3, 5, 7-9, 11-13, 15, 16 and 18-20 have been rejected under 35 U.S.C. 102(b). Claims 4, 6, 10, 14 and 17 have been rejected under 35 U.S.C. 103(a). By this paper, the Applicant amends claims 1, 11, 15, 19 and 20. No new matter has been added.

At ¶2 of the Office Action, the Examiner rejects claims 1-3, 5, 7-9, 11-13, 15, 16 and 18-20 have been rejected under 35 U.S.C. 102(b) as being anticipated by “Efficient Algorithms for Sorting and Synchronization” by Tridgell. The Applicant traverses those rejections. In particular, the Examiner asserts that regarding the limitation, “wherein the cache is part of a storage device,” Tridgell teaches hardware that includes caches and RAM, which are used (i.e., store values) to speed processing. In the “Response to Arguments” at page 8 of the Office Action, the Examiner asserts that the CPU the cache is allegedly part of is a storage device. The Examiner also states that the CPU alone is a “storage device” and the hardware ultimately containing the cache is a “storage device.” The Applicant respectfully submits that one skilled in the art would not characterize a CPU or hardware containing the type of cache taught by Tridgell as a “storage device.” A CPU is a processing device. The fact that a processing device includes memory such as cache, registers and RAM to facilitate its processing functions does not render it a storage device.

To expedite prosecution, however, the Applicant amends independent claims 1, 11, 15, 19 and 20 to recite, “wherein the cache is part of a non-volatile storage device”. Support for this amendment may be found throughout the specification, for example at page 5, line 23 to page 6, line 5, page 10, lines 9-11, and FIG. 1, which describes a disk-based cache. A cache that is part of a “non-volatile storage device” clearly excludes the CPU based cache taught by Tridgell, which will lose its contents when power is removed from the CPU. Tridgell teaches CPU-based cache throughout the reference, and does not teach or suggest cache that is part of a non-volatile storage device.

As amended, independent claims 1, 11, 15, 19 and 20 should be allowable, at least because Tridgell does not teach or suggest cache that is part of a non-volatile memory device. Remaining

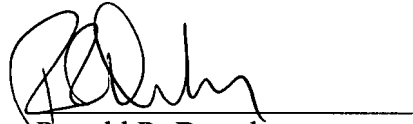
claims 2-10, 12-14 and 16-18 should also be allowable since they depend from allowable base claims.

The statutory period for response expires on August 16, 2007. Accordingly, Applicant respectfully submits that this response is being timely filed.

In view of the above amendment, applicant believes the pending application is in condition for allowance. No other fees are believed to be due in connection with the filing of this response, however the Commissioner is authorized to debit Deposit Account No. 08-0219 for any required fee necessary to maintain the pendency of this application.

Respectfully submitted,

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